

#4/1-9-015
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kim, et al.

Docket No: TI-29012

Serial No: 09/574,653

Examiner: E. Ortiz

Conf. No: 8503

Art Unit: 2815

Filed: 05/18/2000

For: A TUNABLE SIDEWALL SPACER PROCESS FOR CMOS INTEGRATED CIRCUITS

ELECTION

Assistant Commissioner for Patents
Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on 10-26-01.

Ann Trent
Ann Trent

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Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed October 2, 2001.

Applicants hereby elect to pursue Group I of Claims 1-12, drawn to a CMOS integrated circuit, without traversing the Examiner's restriction requirement.

Respectfully submitted,

Peter K. McLarty
Agent for Applicants
Reg. No. 44,923

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